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Multi Objective Analysis of Standard Cells Using Sense Amplifier Based QDI Approach

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Abstract: *The main aim of this paper is to design various Quasi- Delay-Insensitive (QDI) Standard Cell Templates with more energy efficient techniques for asynchronous Circuit design. Out of these, Pre-Charged Half-Buffer (PCHB), Autonomous signal validity Half Buffer(ASVHB) and Sense Amplifier Half-Buffer (SAHB) cell design approaches are probable preferences for low power dissipation ,high speed of operation and high energy efficiency. The first cell design approach is Pre-Charged Half Buffer (PCHB) based on the use of domino logic; however it takes 74% transistor count in the circuit. The second design approach, ASVHB is an asynchronous QDI cell template operates at sub-threshold voltage for low power dissipation. The third design technique, SAHB is an asynchronous QDI cell template used to achieve high speed of operation and low energy and power dissipation. This paper presents seven library cells (i.e., a single input buffer, 2-input AND/NAND, 2-input XOR/XNOR, and 3-input AO/AOI) integrates PCHB, ASVHB, and SAHB design approaches. All the seven library cells are designed and implemented using mentor graphics 130nm technology. The performance attributes like delay, power dissipation,rise time,fall time,duty cycle, slewrate and energy are calculated and tabulated. It also promotes each template with precise characteristics that can be appropriate for low power and high-performance applications.*

Keywords: *Pre-charged Half-Buffer (PCHB); Autonomous Signal-Validity Half-Buffer (ASVHB); Sense Amplifier Half- Buffer (SAHB); Quasi-Delay-Insensitive (QDI); Power dissipation; Rise time; Fall time; Duty cycle; Delay; Slew rate and Energy*

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I. Introduction

Asynchronous design is a more increasingly attractive option compared to synchronous design as it produces high-speed, low-power dissipation, and closer instance to advertise [1]. The significant attempt caused by synchronous system designs are clock skew, power dissipation, interfacing complexity and worst-case performance.QDI design [2] is a level-headed estimate to DI design. An asynchronous communication channel has bunch of wires and a handshake protocol to transfer information between a sender and a receiver [3]. Handshake protocols are divided into two types, one of the handshake protocol is 4 phase protocol and delay insensitivity is accomplished by applying dual-rail encoding scheme, which has two set of wires indicates a single data bit [4]. QDI [2] circuits are free from error for arbitrary wire delays and isochronic forks are pretended for different branches [5]. QDI async approach maintains completion detection mechanism, moreover, it is more feasible and to restrain unknown PVT variations[6-9]. In this paper, we are going to design and implement some of the standard library cells using PCHB[9], ASVHB[10] and SAHB[11] techniques which integrates async QDI logic. These standard cells dissipates less power and more energy efficient and more robust than static CMOS standard cells.

The rest of this paper is organized as follows. Section 2 presents Pre-charged half-buffer, and how standard cells are designed using this approach. Section 3 describes Autonomous signal validity half buffer approach and library cells employed by this approach. Section 4 introduces library cells by making use of SAHB approach. Section 5 delineates presents simulation results and analysis of all the above techniques and their parameters are tabulated. Ultimately, we conclude this paper in section 6.

II. Pre-Charged Half Buffer Template

Pre-Charged Half-Buffer (PCHB) [9] based on the use of domino logic. Usually, PCHB [9, 12] realization approach is an integrated gate-level 4 phase pipeline dual-rail circuit realization. It consists of 2 handshake signals named as R_{ack}(acknowledge-in) and L_{ack} (acknowledge-out) and en is an internal signal which is integrated into a microcell. The pre-charged half-buffer structure has 2 completion detectors arranged at both

sides of the input and output which are accustomed to validate the availability of input/output. Figure 1 shows the circuit schematic of a buffer embodying PCHB approach. The buffer cell including PCHB is operated as follows. First of all, set all the data input(A.T/A.F) and data output(Q.T/Q.F) is empty(i.e., logic '0'); the handshake signals (L_{ack} & R_{ack}), the control signal (En) and intermediate outputs are placed at logic '1'.When valid data input is applied , the pull-down network evaluates the functional block which provides valid data output by emphasizing S.T/ S.F . Now the completion of evaluation is acknowledged by setting L_{ack} & En to logic'0' through ICD/OCD. When data input & output are empty (R_{ack} to logic '0') then ICD/OCD reasserts Lack & En to logic"1". After reset operation, a new process of the cell can be started by setting R_{ack} to logic'1'. For a proper operation of the template, data output should be reset to logic '0'.

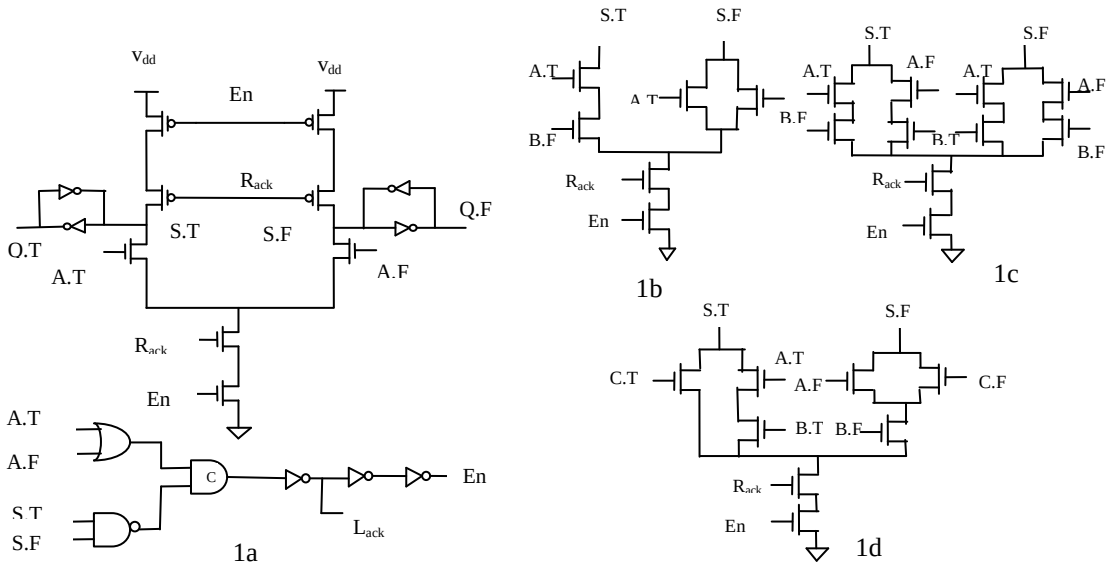


Figure 1. Standard cells embodying PCHB approach (a) single input buffer (b) 2-input AND/NAND (c) XOR/XNOR (d) 3-input AO/AOI

In order to crush the overhead of high power dissipation, we are going for ASVHB design approach discussed below.

III. Autonomous Signal Validity Half-Buffer

The realization of Autonomous signal-validity half-buffer (ASVHB) [10] approach is an Asynchronous-logic quasi-delay insensitive (QDI) cell template for low power sub-threshold operation (VDD = 0.2 V). For ease of understanding of ASVHB realization approach, we are explaining a single-input BUFFER cell shown in Figure 2. The ASVHB functional block has two sub-blocks named as 'true' rail sub-block and a 'false' rail sub-block

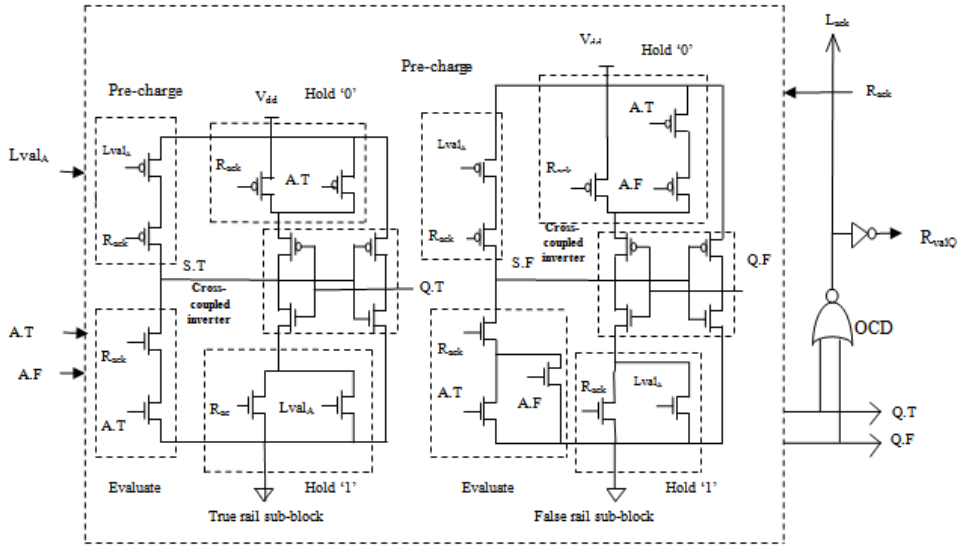


Figure 2 ASVHB single-input buffer

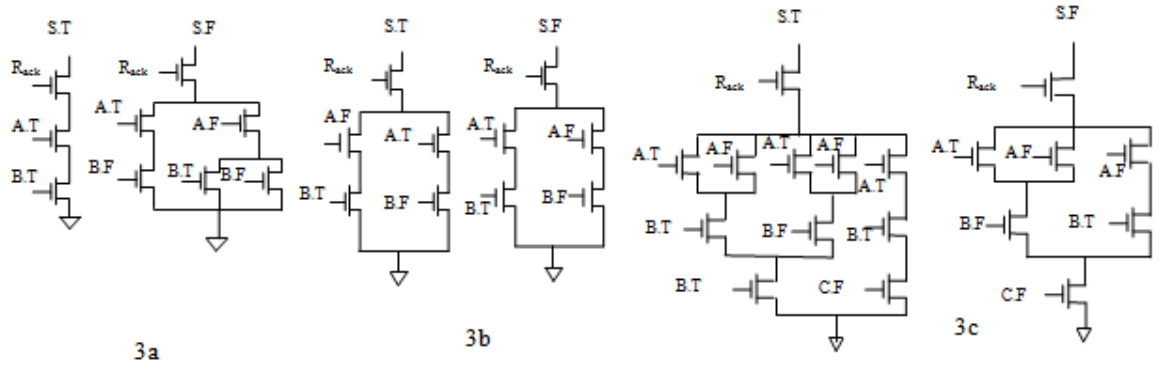


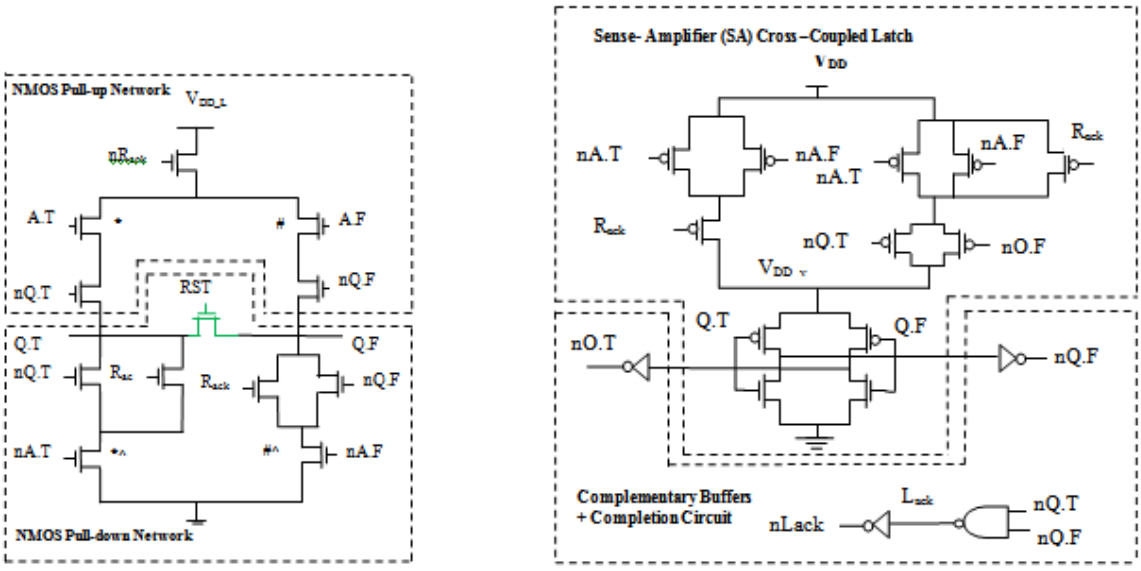
Figure 3: standard cells embodying ASVHB approach (a) AND/NAND (b) XOR/XNOR (c) AO/AOI.

The operation of ASVHB Buffer cell is as follows. Initially, all the input data signal (A.T/A.F) the output data signal (Q.T/Q.F) is at logic '0', the acknowledge signals (L_{ack} and R_{ack}) and the intermediate data (S.T/S.F) are at logic '1'.In Evaluation phase, when the data input A.T = '1' (A.F = '0'), S.T will become '0' and Q.T will be logic '1. For completeness of input L_{ack} is negated to '0' through OCD. For output completeness, further $Rval_Q$ is triggered to logic '1, this represents a valid output and R_{ack} will be negated to logic '0.

During the pre-charge phase, When the inputs are pre-charged at preceding pipeline then L_{valA} is reset to logic '0', S.T will become '1' (through the 'pre-charge' section), and Q.T is discharged to logic '0' (through the cross-coupled inverter). At last, the ASVHB cell is prepared for a new operation.

IV. Sense Amplifier Half-Buffer

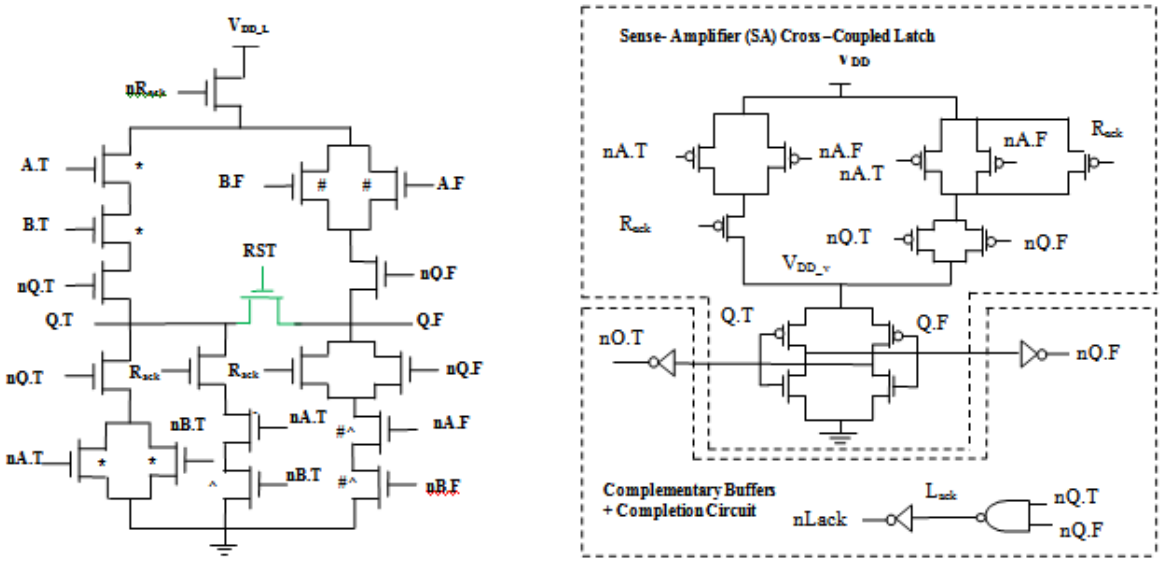
The SAHB [11] cell uses async 4-phase handshake protocol [4] which has two alternate operation sequences referred to as evaluation and reset. For the design, Figure 4(a) and (b) shows the circuit schematic of a SAHB buffer cell contains an evaluation block and an SA block [14]; the blocks within the dotted lines are the versatile sub-blocks. For the initialization of cell, the nMOS transistor in green denoted with RST is subjugated which is optional. Figure 4 shows a single-input buffer, the transistor constellation of the primary input A.T/A.F in the pull-up network is a series-parallel analysis to the transistor constellation of nA.T/nA.F in the pull-down network. Q.T and Q.F path of the series-parallel pairs are distinguished with * and # respectively.



4 (a) **4(b)**

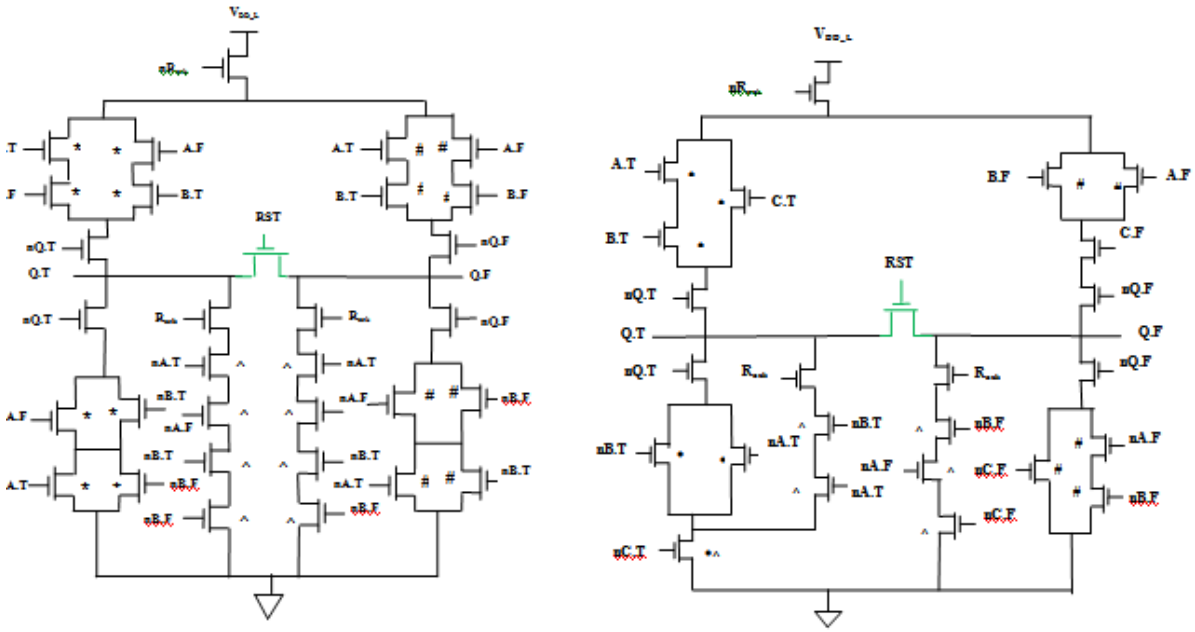
*, # Series-Parallel Pair ^ Input-completeness

Figure 4(a). Evaluation block of a buffer cell (b) SA block of a buffer cell embodying SAHB powered by $V_{DD.}$
In Figure 4(a) and (b), R_{ack} is evaluation flow control signal and nR_{ack} is known as reset flow control signal. In Figure 4(b), the SA block is a combination of the cross-coupled latch, complementary buffers, and a completion circuit.



5(a)

At first, all the inputs reset to 0 and their respective complementary signals are set to 1. For example, we first consider A.F=1 (nA.F=0) in the evaluation phase, the nMOS pull-up network partially charges the voltage at Q.F to V_{DD_L} and Q.T remains 0. As the applied input is valid, SA cross-coupled latch turns on due to the direct connection of V_{DD_v} to V_{DD} and magnifies Q.F to 1. Consequently, Q.F is latched and nQ.F becomes 0. The dual-rail output is valid by charging L_{ack} to 1 (nL_{ack} =0).



5(b) **5(c)**

Figure 5: standard cells embodying SAHB approach (a) AND/NAND (b) XOR/XNOR (c) AO/AOI.

During the reset phase, the dual-rail output is empty as the empty input (nA.T and nA.F are 1) is applied and L_{ack} is obtained as 0. As a result, the new operation of SA [11, 13] block can be performed. At last, both the evaluation block and SA block are tightly connected to each other to diminish the number of switching nodes, so it enhances the high speed and decreases the power dissipation [14]. The input signals A.T and A.F with input completeness [9] and handshake signal R_{ack} (nR_{ack}) acknowledges the evaluation block, so it is said to be gate-orphan-free. Simulation results and analysis of all the Library cells are discussed in section 5. Figure 5 shows the library cells using Sense Amplifier Half-Buffer approach. Next section delineates the simulation results and waveforms of all the library cells embodying three different approaches.

V. Simulation Results And Discussions

Figure 6 depicts Schematic and simulated waveforms of Buffer cell embodying PCHB approach.

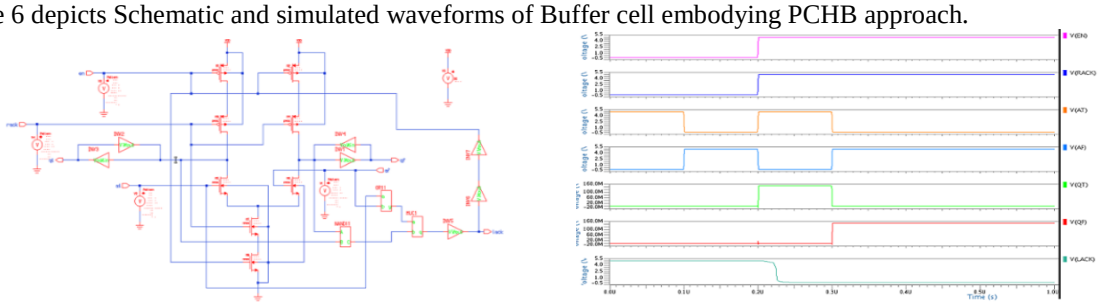


Figure 6. Schematic and simulated waveforms of Buffer cell embodying PCHB approach

Similarly, Figure 7 shows Schematic and simulated waveforms AND cell embodying PCHB approach

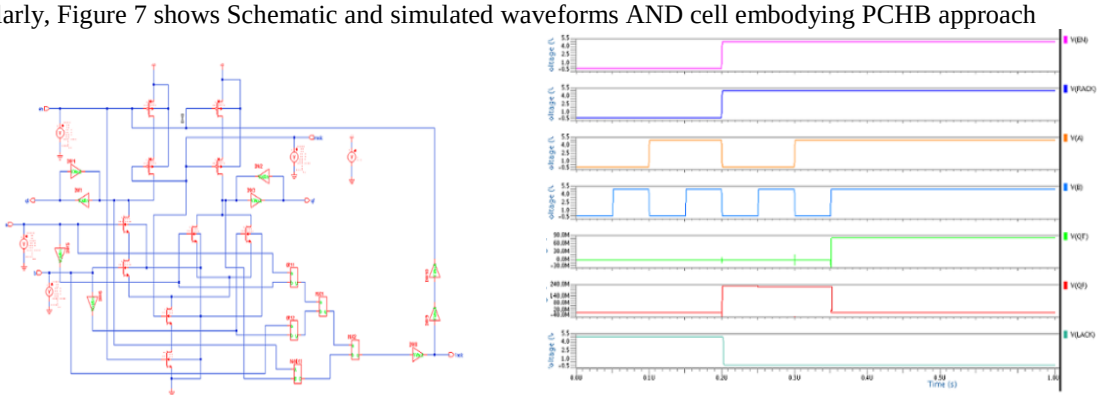


Figure 7. Schematic and simulated waveforms AND cell embodying PCHB approach

Figure 8 shows the Schematic and simulated waveforms of XOR cell embodying PCHB approach

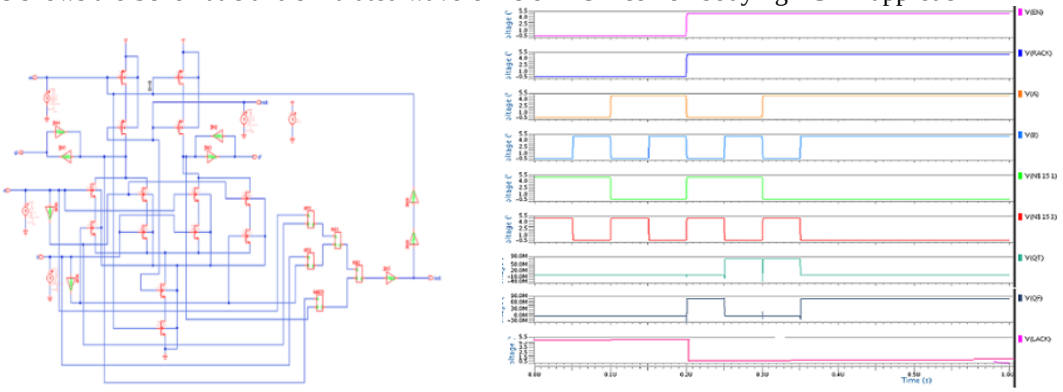


Figure 8.Schematic and simulated waveforms of XOR cell embodying PCHB approach

Similarly, Figure 9 depicts Schematic and simulated waveforms of AO gate embodying PCHB approach

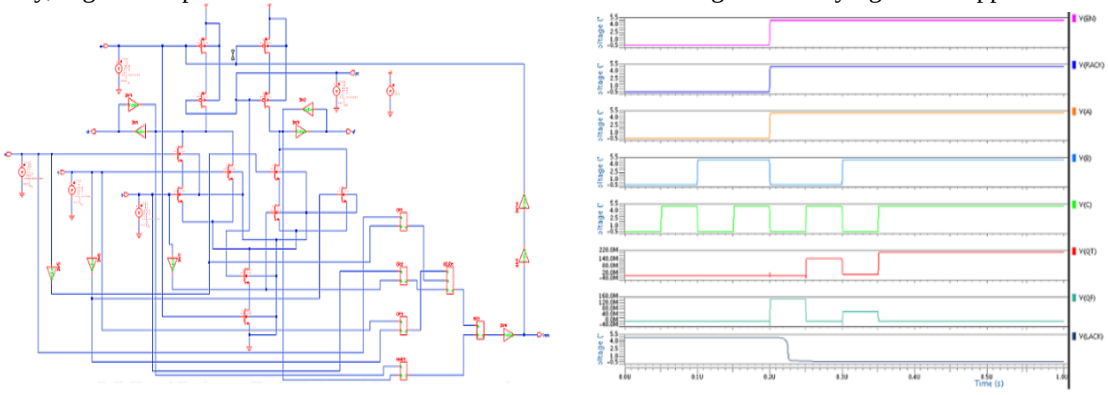


Figure 9. Schematic and simulated waveforms of AO gate embodying PCHB approach

Figure 10 depicts Schematic and simulated waveforms of Buffer cell embodying ASVHB approach

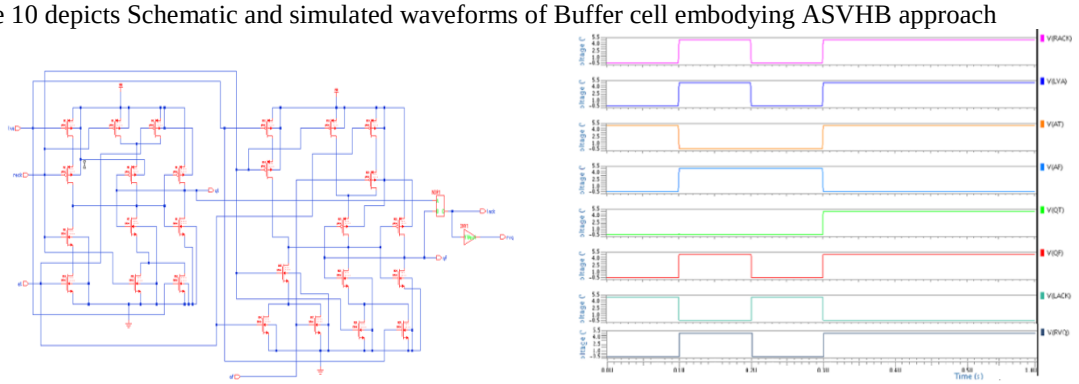


Figure 10.Schematic and simulated waveforms of Buffer cell embodying ASVHB approach

Similarly, Figure 11 shows Schematic and simulated waveforms AND cell embodying ASVHB approach

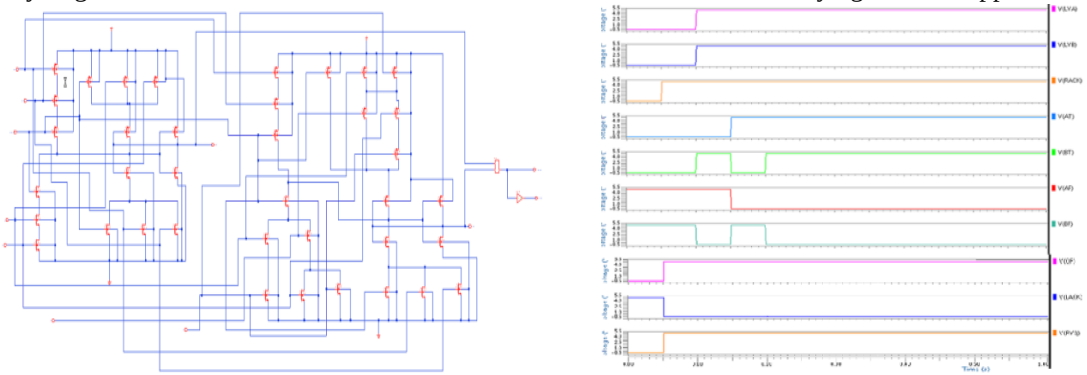


Figure 11. Schematic and simulated waveforms AND cell embodying ASVHB approach

Below figure shows the schematic and simulated waveforms of XOR cell embodying ASVHB approach

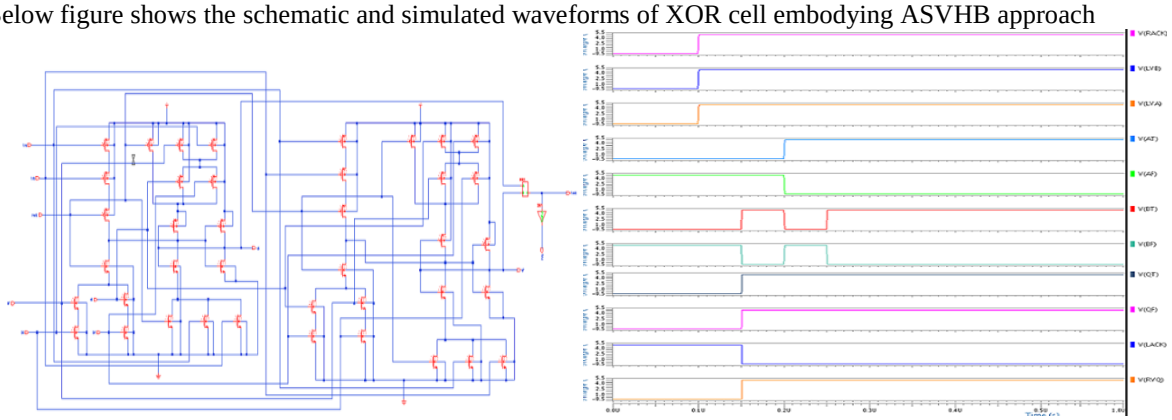


Figure 12.schematic and simulated waveforms of XOR cell embodying ASVHB approach

Below figure depicts Schematic and simulated waveforms of AO cell embodying ASVHB approach

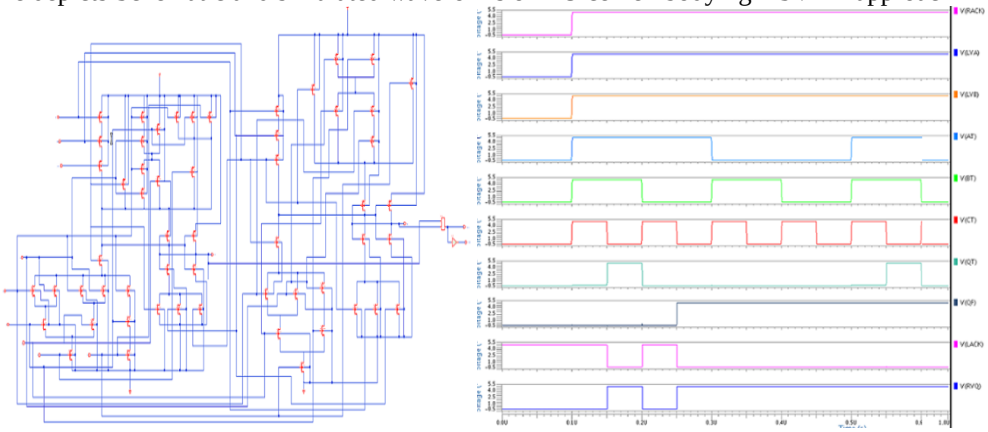


Figure 13. Schematic and simulated waveforms of AO cell embodying ASVHB approach

Circuit schematic and simulated waveforms of buffer cell embodying SAHB approach are shown in figure 14

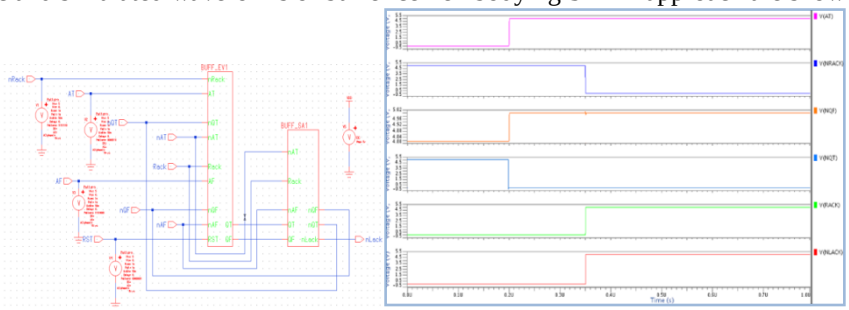


Figure 14.schematic and simulated waveforms of buffer cell embodying SAHB approach

Circuit schematic and simulated waveforms AND cell embodying SAHB approach are shown in figure 15

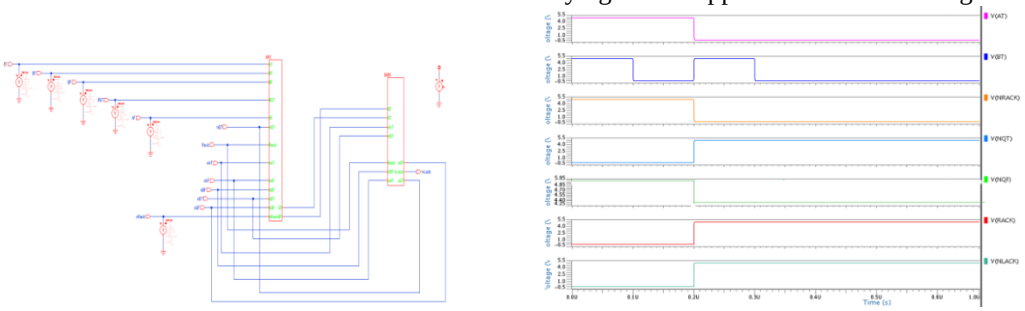


Figure 15.schematic and simulated waveforms AND cell embodying SAHB approach

Figure 16 depicts schematic and simulated waveforms of XOR cell embodying SAHB approach

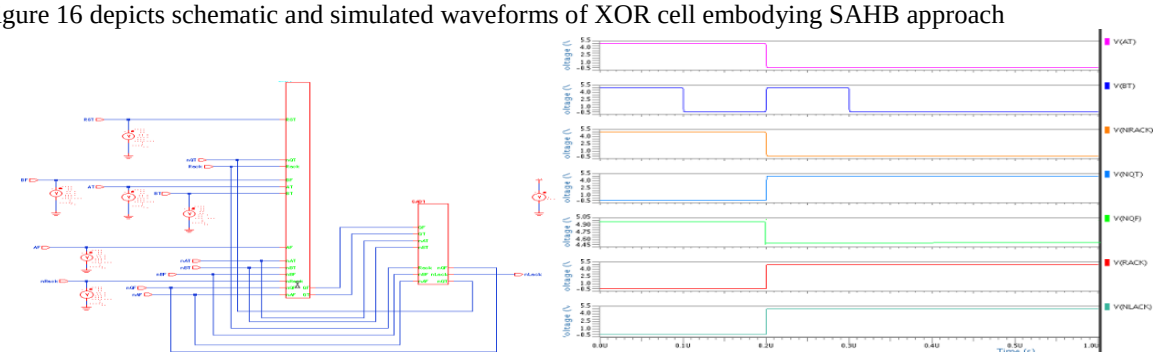


Figure 16.schematic and simulated waveforms of XOR cell embodying SAHB approach

Circuit Schematic and simulated waveforms of AO cell embodying SAHB approach are shown in figure 17

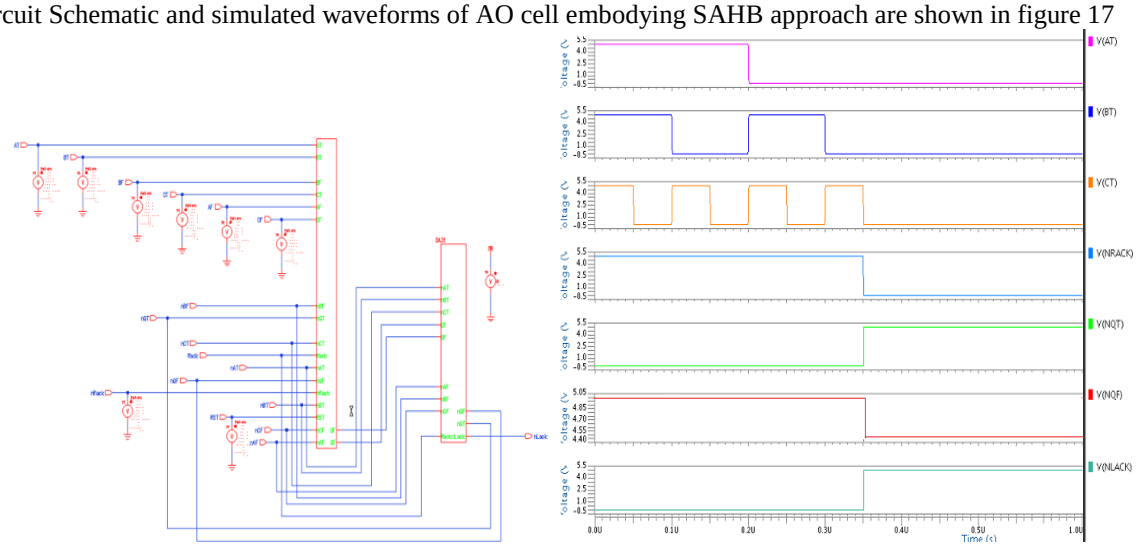


Figure 17. Schematic and simulated waveforms of AO cell embodying SAHB approach

Parameters of Various LIBRARY CELLS EMBODYING PCHB, ASVHB, and SAHB are tabulated in Table I. Based on the simulations, Table I reveals the power dissipation, delay, energy (power x delay),rise time, fall time, and slew rate of 7 cell templates of three different approaches.

TABLE I
Parameters of Various LIBRARY CELLS EMBODYING PCHB, ASVHB, and SAHB

S.no	Parameters	1-inputBuffer			2-input AND/NAND			2-input XOR/XNOR			3-input AO/AOI		
		PCHB	ASVHB	SAHB	PCHB	ASVHB	SAHB	PCHB	ASVHB	SAHB	PCHB	ASVHB	SAHB
1	Power(nw)	13.1	13.05	7.38	13.2	13.1	5. 26	13.4	12.9	5.24	13.5	13.6	5.31
2	Delay(ps)	221	205.7	180	340	123.79	320	301	167.86	343	302	132.4	340.8
3	Risetime(ps)	385	514.2	714	387	520.6	720	392	536.9	724	402	540.8	726.3
4	Fall time(ps)	477	627.8	402	480	630.2	403	482	632.9	410	490	640.5	420.6
5	Slew rate(G)	16.7	28.92	31	16.5	28.7	31.4	16.8	28.6	32.7	16.9	29.5	32.4
6	Energy(uj)	4650	2648	1330	3348	1764	1686	3467	2030	1547	2189	1808	1760

For simplicity of elucidation, the attributes of the different library cells are standardized with respect to their resultant SAHB cell templates whose concrete values are exposed inside the parenthesis. The typical characteristics of the seven library cells are tabularized in the last row of Table I.

VI. Conclusions And Future Work

In this paper, we have designed and implemented standard cells using three design approaches such as PCHB, ASVHB, and SAHB techniques. From the table I, we can conclude that out of three design approaches, SAHB dissipates less power, more robust and high energy efficiency. The 7 library cells (i.e., 1-input Buffer, 2-input AND/NAND, 2-input XOR/XNOR, 3-input AO/AOI) embodying PCHB, ASVHB, and SAHB are designed and implemented in section III and their simulated waveforms are depicted in section IV. Several characteristics of all the three approaches library cells are compared and tabulated in Table I.As a result, the library cells embodying SAHB, on average, dissipate ~25% lower power and ~23% lower energy than remaining approaches. Further reduction in delay and power dissipation can be performed with the technologies like GALEOR and LECTOR algorithm.

Acknowledgements

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